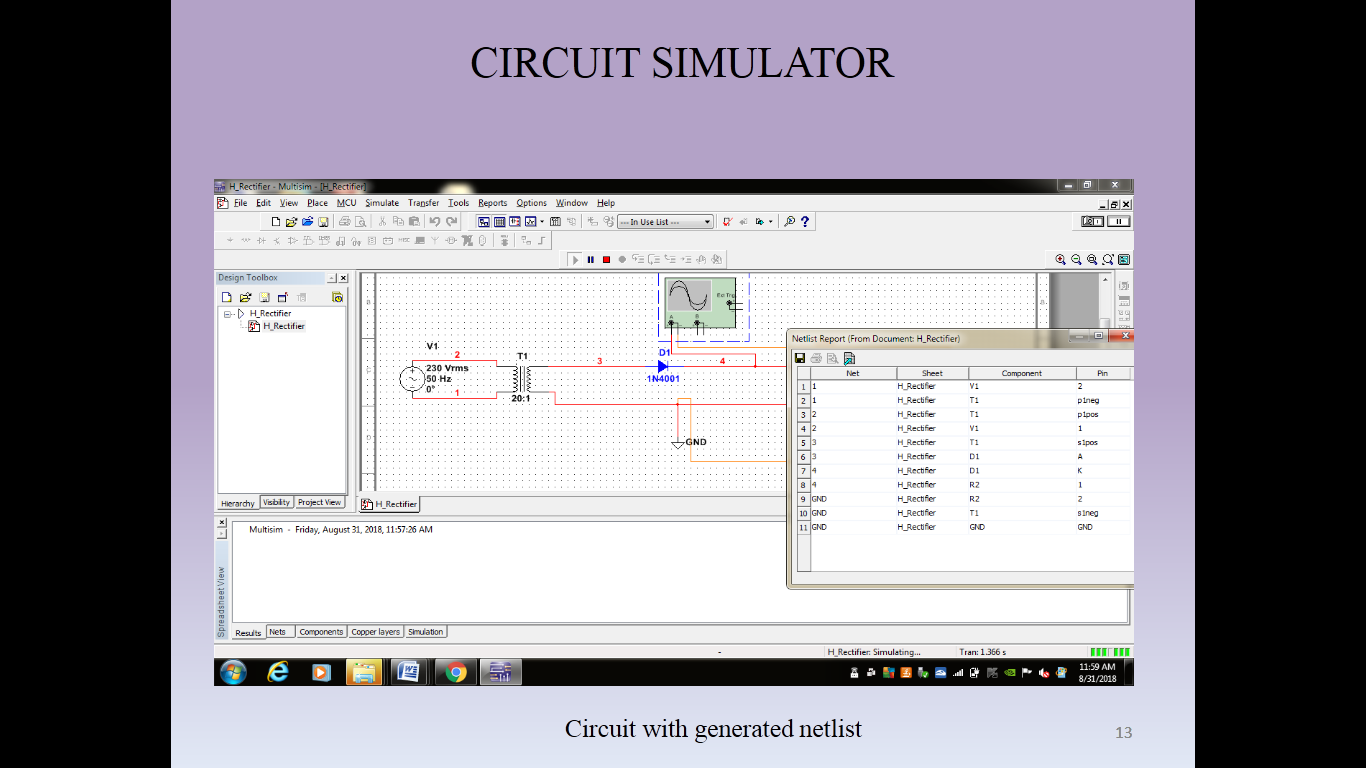
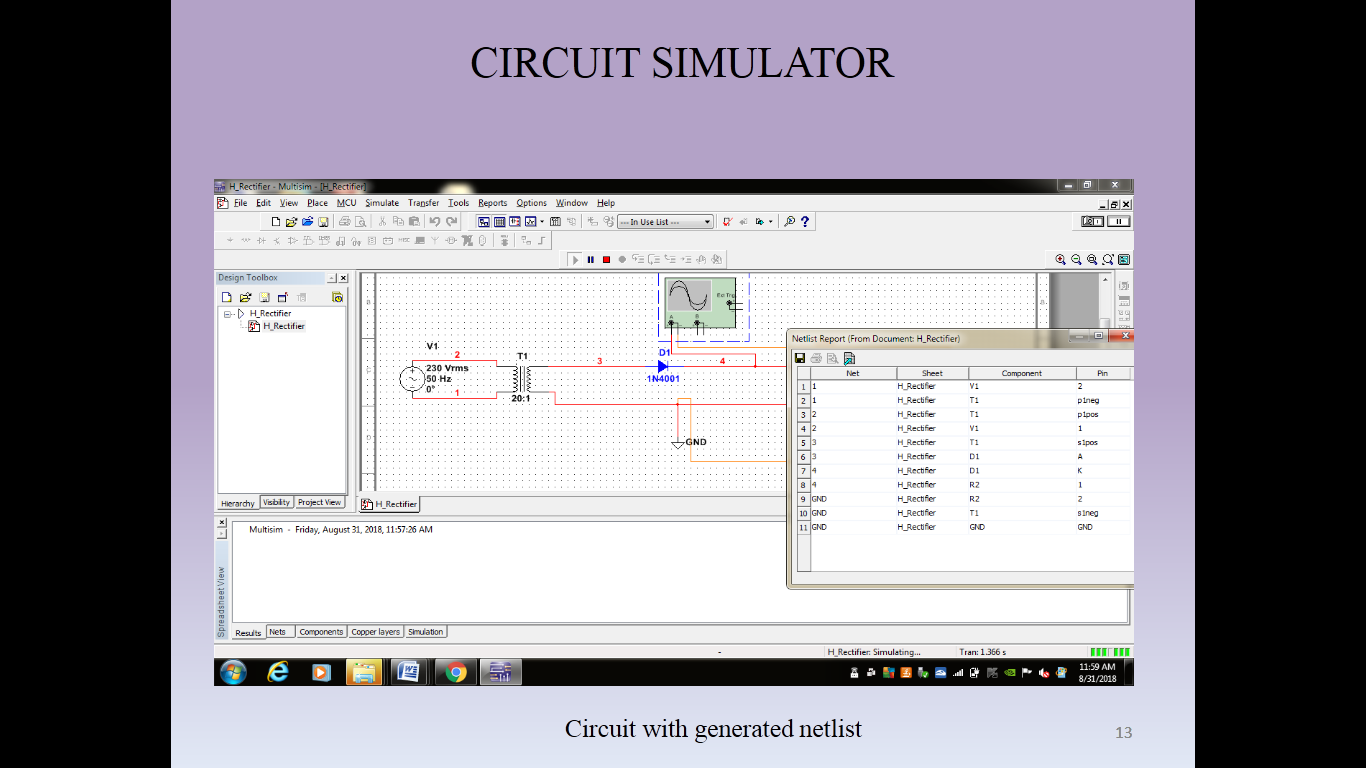
DOCUMENTATION ON MAPPING TABLE

**1.1 Multisim tool simulation for HWR circuit(with Netlist)**





**1.2 Notation representation table for pins of the components**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bread board notation | Pin No.(LHS) | Component | Pin No.(RHS) | Bread board notation |
| A1 | 1 | Diode | 2 | B1 |
| A2 | 1 | Resistor | 2 | B2 |
| A3 | 1 | Transformer | 2 | B3 |
| A4 | 1 | Voltage source | 2 | B4 |
| A5 |  | Ground |  | B5 |

**1.3 Mapping table(for HWR)**

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|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bread board notation | A1 | A2 | A3 | A4 | A5 | B1 | B2 | B3 | B4 | B5 |
| Netlist notation | D1 A | R2 1 | T1 P1 Pos | V1 1 | GND | D1 K | R2 2 | T1 P1 Neg | V1 2 | GND |
| Node number | 3 | 4 | 2 | 2 | GND | 4 | GND | 1 | 1 | GND |